Listing of Claims

1. (Currently Amended) A method for manufacturing non-volatile memory cells on a semiconductive substrate, comprising at least the following steps:

forming active areas in said semiconductive substrate, bounded by portions of an insulating layer;

forming a first thin layer of tunnel oxide and depositing a first layer of conductive material on said active areas;

defining a plurality of floating gate regions, wherein the definition of the floating gate regions comprises the steps of:

forming a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes;

forming spacers of a second material in the shelter of the side walls of said stripes, said second material being selectively etchable with respect to said first material,

depositing a layer of a third material in order to fill in the space between said spacers,

polishing said layer of a third material together with said alternated stripes and said spacers to ~~substantially~~ the same planar level,

selectively removing said spacers in order to expose portions of said first layer of semiconductive material,

etching said first layer of semiconductive material in order to form grooves in correspondence with its exposed portions,

selectively removing said alternated stripes and said layer of a third material.

2. (Original) The method according to claim 1, wherein said first material and said third material are a conductive material.

3. (Original) The method according to claim 2, wherein said plurality of alternated stripes is formed by depositing a second layer of conductive material and by defining said second layer of conductive material by means of lithography.

4. (Original) The method according to claim 3, wherein between said first layer of semiconductive material and said second layer of semiconductive material a thin oxide layer is interposed.

5. (Original) The method according to claim 1, wherein said second material is silicon nitride and wherein the formation of said spacers in the shelter of the side walls of said alternated stripes comprises the deposition of a silicon nitride layer, which is patterned by means of an anisotropic etching.

6. (Original) The method according to claim 1, wherein said first material and said third material are each an oxide.

7. (Original) The method according to claim 6, wherein said plurality of alternated stripes is formed by depositing a first oxide layer and by defining said first oxide layer by means of lithography.

8. (Original) The method according to claim 7, wherein said second material is silicon nitride and wherein the formation of said spacers in the shelter of the side walls of said alternated stripes comprises the deposition of a silicon nitride layer, which is patterned by means of an anisothropic etching.

Claims 9-13. (Canceled).

14. (Currently Amended) A method for manufacturing non-volatile memory cells on a semiconductor substrate, comprising:

forming active areas in said semiconductor substrate, bounded by portions of an insulating layer;

depositing a first thin layer of tunnel oxide and a first layer of conductive material on said active areas; and

defining a plurality of floating gate regions, comprising:

forming stripes of shielding material only above pairs of alternated active areas;

defining spacers of small width in the shelter of the side walls of the stripes thus defined;

defining stripes of shielding material also on the active areas that lacked them;

polishing the stripes and spacers to ~~substantially~~ the same planar level;

removing the spacers to form openings; and

etching the first layer of conductive material through the openings to form a plurality of gate regions.

15. (Currently Amended) A semiconductor fabrication method, comprising:

forming a plurality of first stripes from a polysilicon material over an insulated base polysilicon layer and which lie above first alternating active areas;

forming sidewall spacers for the plurality of first stripes;

forming a plurality of second stripes from a polysilicon material between the sidewall spacers over the insulated base polysilicon layer which lie above second alternating active areas;

chemically mechanically polishing the first stripes, second stripes and sidewall spacers to ~~substantially~~ the same planar level; and

removing the sidewall spacers.

16. (Currently Amended) The method according to Claim 15, wherein forming the plurality of first stripes comprises:

depositing a first polysilicon material layer;

defining the first stripes in the first material layer using a photolithography mask;

etching using the mask to remove the first material layer but leave the first stripes.

17. (Currently Amended) The method according to Claim 15, wherein forming the plurality of second stripes comprises:

depositing a second polysilicon material layer that covers the first stripes and fills a region between sidewall spacers.

18. (Original) The method according to claim 15, wherein forming sidewall spacers comprises:

depositing a nitride layer; and

patterning the nitride layer to remove the nitride layer above the second alternating active areas but leave the nitride layer adjacent sidewalls of the first stripes.

19. (Original) The method according to Claim 15, further comprising:

using the first and second stripes as a hard mask; and

etching using the first and second stripes hard mask to define floating gate regions in the base polysilicon layer above both the first and second alternating active areas.

20-21. (Canceled).

22. (Currently Amended) A method for semiconductor fabrication on a substrate including a plurality of active areas, comprising:

forming a plurality of first polysilicon stripes by photolithographic techniques over an insulated base polysilicon layer and which lie above even ones of the plurality of active areas; and

forming a plurality of second polysilicon stripes without the use of photolithographic techniques over the insulated base polysilicon layer and which lie above odd ones of the plurality of active areas;

wherein the plurality of first and second polysilicon stripes have a polished upper surface at ~~substantially~~ the same planar level.

23. (Currently Amended) The method of claim 22 wherein forming a plurality of first polysilicon stripes comprises:

depositing a first polysilicon material layer;

defining the first polysilicon stripes in the first material layer using a photolithography mask;

etching using the mask to remove the first material layer but leave the first polysilicon stripes.

24. (Currently Amended) The method of claim 22 wherein forming the plurality of second polysilicon stripes comprises:

forming sidewall spacers for the plurality of first polysilicon stripes;

forming the plurality of second polysilicon stripes between the sidewall spacers over odd ones of the active areas; and

removing the sidewall spacers.

25. (Currently Amended) The method of claim 22 wherein forming the plurality of second polysilicon stripes comprises:

forming sidewall spacers for the plurality of first polysilicon stripes;

depositing a second polysilicon material layer that covers the first polysilicon stripes and fills a region between the sidewall spacers;

chemically mechanically polishing to remove the second material layer but leave the second polysilicon stripes such that the first and second polysilicon stripes have the polished upper surface at ~~substantially~~ the same level.

26. (Currently Amended) The method according to claim 22, wherein forming sidewall spacers comprises:

depositing a nitride layer; and

patterning the nitride layer to remove the nitride layer above odd ones of the active areas but leave the nitride layer adjacent sidewalls of the first polysilicon stripes.

27. (Currently Amended) The method according to Claim 22, further comprising:

using the first and second polysilicon stripes as a hard mask; and

etching using the first and second polysilicon stripes hard mask to define floating gate regions in the base polysilicon layer above both the odd and even ones of the active areas.

Claims 28-33. (Canceled).